

# AREA EFFICIENT FIXED-WIDTH BOOTH MULTIPLIERS WITH HIGH ACCURACY

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**ABSTRACT**-In this project a single compensation formula of adaptive conditional-probability estimator (ACPE) applied to fixed-width Booth multiplier is proposed. Based on the conditional- probability theory, the ACPE can be easily applied to large length Booth multipliers (such as 32-bit or larger) for achieving a higher accuracy performance. To consider the trade-off between accuracy and area cost, the ACPE provides varying column information  $w$  to adjust the accuracy with respect to system requirements.

The 16-bit ACPE Booth multiplier with  $w = 3$  reduces 28.9% silicon area with only 0.39 dB signal-to-noise ratio (SNR) loss when compared with post-truncated (P-T) Booth multiplier. Furthermore, the ACPE Booth multipliers are applied to two-dimensional (2-D) discrete cosine transform (DCT) to evaluate the system performance. Implemented in a TSMC 0.18  $\mu$ m CMOS process, the DCT core with ACPE ( $w = 3$ ) can save 14.3% area cost with only 0.48 dB peak-signal-to-noise-ratio (PSNR) penalty compared to P-T method. According to the applications of larger bit width fixed-width multipliers, like pseudo random number generator (PRNG), huge number of time will be consumed to establish the compensation function based on exhaustive simulation. Therefore, a compensation function is presented in binary-sign-digit (BSD) Booth multipliers by using condition-probability method.

The conditional bits in are not chosen well. Thus, the compensation circuits cannot improve the performance in accuracy when compared with existing works. The probabilistic estimation bias is presented to replace the time-consuming exhaustive simulation methods and it also exhibits good accuracy performance.

**INDEX TERMS**-Adaptive conditional-Probability estimator(ACPE), Booth multiplier, Discrete cosine transform (DCT),fixed-width.

## 1.INTRODUCTION

FIXED-WIDTH multipliers are the important components in digital signal processing (DSP) systems . In general, they truncate the least significant half part directly to generate the output with the same word length as input, and the computation errors occur from the operators that perform the truncation. Therefore, many compensation methods are presented to reduce the truncation errors in Baugh-Wooley array multipliers and Booth multipliers.

Booth multipliers are popular due to the reduced elements of the partial products. The fixed-width Booth multiplier with the best accuracy is the post-truncated (P-T) multiplier, which uses rounding off operator after calculating all products. However, the P-T multiplier consumes large silicon area in very large scale integration (VLSI) designs. In order to reduce the area cost, the direct-truncated (D-T) multiplier chops the least significant half partial products directly.

Recently, many works use more information from Booth encoder and partial products to achieve higher accuracy performance. In , taking more information provided by Booth encoder, the compensation circuits can reduce the truncation errors. Wang *et al.* further improve the work of truncation errors can be alleviated evidently. Nevertheless, the area cost is increased from the extra information of compensation circuits.

There is a trade-off between accuracy and area cost. Song *et al.* introduce the column information to provide more choices between accuracy and area cost . The compensation function is also established by the exhaustive simulation to adjust the accuracy with respect to system requirements based on varying . In this paper, a high-accuracy adaptive conditional-probability estimator (ACPE) is proposed to be applied in fixed-width Booth multipliers.

Instead of the time-consuming exhaustive simulation of the previous works, the ACPE is derived from the conditional-probability theory.

Thus, the ACPE can be easily applied to large length Booth multipliers (such as 32-bit or larger).

**1.1 BOOTH'S MULTIPLIER:**

Booth multiplier will multiply  $a \cdot b$  where  $a$  is multiplicand and  $b$  is multiplier. The key to Booth's insight is to divide the groups bit of multiplier into 3 parts: the beginning, the middle, or the end of a run of 1s.

In general, truncate the least significant half part directly to generate the output with the same word length as input, and the computation errors occur from the operators that perform the truncation. Booth multipliers are popular due to the reduced elements of the partial products. In this paper, a high-accuracy adaptive conditional-probability estimator (ACPE) is proposed to be applied in fixed-width Booth multipliers. Thus, the ACPE can be easily applied to large length Booth multipliers (such as 32-bit or larger). Requirements, the ACPE also provide varying column information ( $W$ ) to adjust the system accuracy. Furthermore, the ACPE Booth multipliers are also applied to a two-dimensional (2-D) discrete cosine transform (DCT) to demonstrate the performance of real applications.

**1.2 SCOPE OF THE PROJECT:**

In this project, a high-accuracy adaptive conditional-probability estimator (ACPE) is proposed to be applied in fixed-width Booth multipliers. Instead of the time-consuming exhaustive simulation of the previous works, the ACPE is derived from the conditional-probability theory. Thus, the ACPE can be easily applied to large length Booth multipliers (such as 32-bit or larger). As a result, the ACPE can reduce 14.3% area cost compared to P-T method with only 0.48 dB peak-signal-to-noise-ratio (PSNR) lost. Consequently, the proposed ACPE saves the establishment time of compensation circuit, provides varying column information, and achieves the high accuracy performance in a single compensation function.

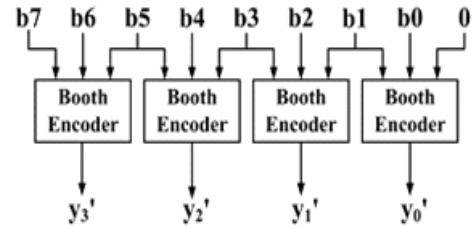


Fig. 1.2 Grouping Bits of Booth Encoder

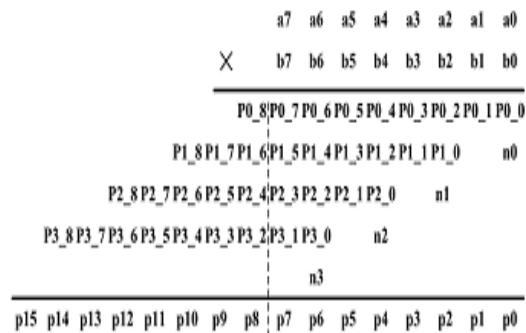
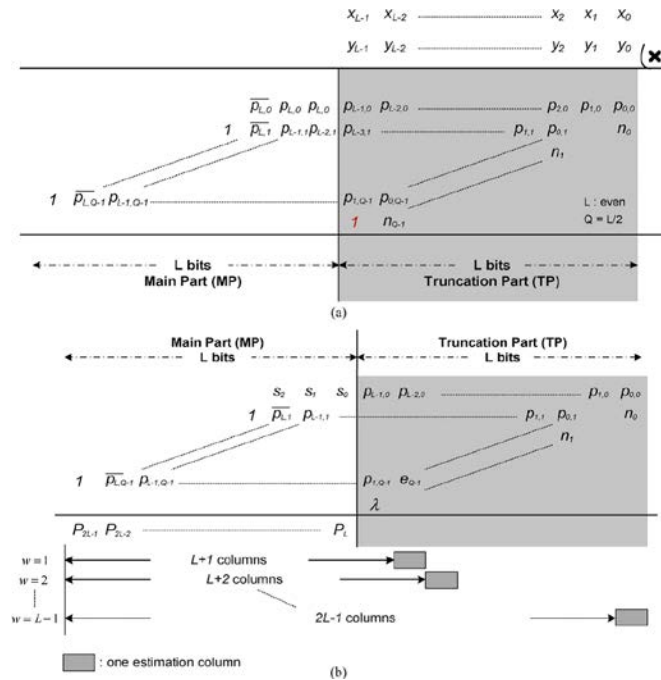


Fig. 1. 1.8-bit Booth Multiplier

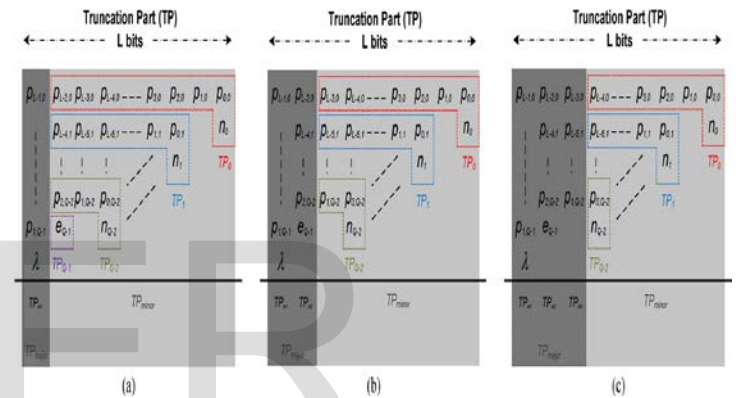
**II. FIXED-WIDTH MODIFIED BOOTH MULTIPLIER**

Modified Booth encoding is popular for reducing the number of partial products. The  $n$ -bit product can be expressed in two's complement representation as follows: (1) Three concatenated inputs,  $b_{2i+1}$ ,  $b_{2i}$ , and  $b_{2i-1}$ , and can be mapped into by using Booth encoder, as tabulated in Table I, where nonzero code is a 1-bit digit whose value is determined by whether  $b_{2i+1}$  equals to zero. There are rows in partial product array producing by Booth encoding, where  $i$  is an even number.



The partial product array also can be divided into two parts: the main part (MP) including the most significant ‘L’ columns, and the truncation part (TP) including the least significant ‘L’ columns. Besides, the column information “w” is included to adjust accuracy with respect to system requirements, and ‘W’ means that most significant columns (MSC) are calculated and the MSC is chosen to estimate the compensation values.

fig.1.3 Truncated parts of lambda=1,2,3.



According to the mapping Tables , Booth encoder will generate the partial products.

| $y_{2i+1}$ | $y_{2i}$ | $y_{2i-1}$ | $y'_i$ | $nz_i$ |
|------------|----------|------------|--------|--------|
| 0          | 0        | 0          | 0      | 0      |
| 0          | 0        | 1          | 1      | 1      |
| 0          | 1        | 0          | 1      | 1      |
| 0          | 1        | 1          | 2      | 1      |
| 1          | 0        | 0          | -2     | 1      |
| 1          | 0        | 1          | -1     | 1      |
| 1          | 1        | 0          | -1     | 1      |
| 1          | 1        | 1          | 0      | 0      |

TABLE 1.1 Modified booth Encoder

| $n_{Q-1}$ | $p_{0,Q-1}$ | $p_{L,0}$ | $s_2$ | $s_1$ | $s_0$ | $\lambda$ | $e_{Q-1}$ |
|-----------|-------------|-----------|-------|-------|-------|-----------|-----------|
| 0         | 0           | 0         | 1     | 0     | 0     | 1         | 0         |
| 0         | 0           | 1         | 0     | 1     | 1     | 1         | 0         |
| 0         | 1           | 0         | 1     | 0     | 0     | 1         | 1         |
| 0         | 1           | 1         | 0     | 1     | 1     | 1         | 1         |
| 1         | 0           | 0         | 1     | 0     | 0     | 1         | 1         |
| 1         | 0           | 1         | 0     | 1     | 1     | 1         | 1         |
| 1         | 1           | 0         | 1     | 0     | 1     | 0         | 0         |
| 1         | 1           | 1         | 1     | 0     | 0     | 0         | 0         |

TABLE 1.2 Modified booth Encoder partial products

## 2.ALGORITHM:

### ADAPTIVE CONDITIONAL-ROBABILITY ESTIMATOR FOR FIXED-WIDTH BOOTH MULTIPLIER

when the multiplier and multiplicand enters the booth encoder according to the table the partial products were computed ad sent to csa tree and compensation circuit and finally all the partial sum and carry products were added at parallel prefix adder unit and pq will be the quantized product

Modified Booth encoding is popular for reducing the number of partial products. The 2L -bit product P can be expressed in two’s complement representation as follows:

$$X = -x_{L-1}2^{L-1} + \dots + x_0$$

$$Y = -y_{L-1}2^{L-1} + \dots + y_0$$

$$P = X \times Y$$

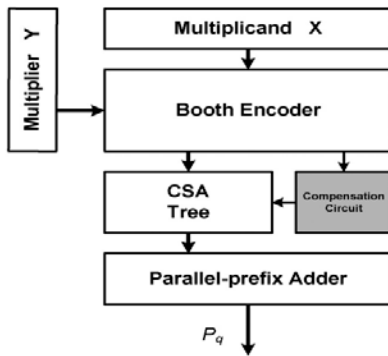


fig 1.4 PROPOSED BLOCK DIAGRAM

Three concatenated inputs  $y_{2i+1}$ ,  $y_{2i}$ , and  $y_{2i-1}$  can be mapped  $y_i$  into by using Booth encoder, as tabulated in Table I, where nonzero code is a 1-bit digit whose value is determined by whether  $y_i$  equals to zero. There are  $Q=L/2$  rows in partial product array producing by Booth encoding, where  $L$  is an even number.

$$\{s_2, s_1, s_0, \lambda, e_{Q-1}\} = \{p_{L,0}, p_{L,0}, p_{L,0}, 1, p_0, Q-1\} + \{0, 0, 0, 0, n_{Q-1}\}$$

The partial product array in Fig. 1(b) also can be divided into two parts: the main part (MP) including the most significant  $L$  columns, and the truncation part (TP) including the least significant  $L$  columns. Besides, the column information  $\omega$  is included to adjust accuracy with respect to system requirements, and  $\omega$  means that  $L + \omega$  most significant columns (MSCs) are calculated and the  $(L + \omega + 1)^{th}$  MSC is chosen to estimate the compensation values. Therefore,  $L + \omega + 1$  MSCs are used to produce the results. Taking  $\omega = 2$  as an example, the results are calculated by the partial products of most significant  $L + 3 (= L + \omega + 1)$  columns.

When fixed-width multiplication is concern, the quantized product  $P_q$  can be expressed as follows:

$$P \approx P_q = MP + TP \\ = MP + \sigma 2^L \dots \dots \dots (a)$$

Where  $\sigma$  represents the bias of adaptive conditional-probability estimator (ACPE) which can be decomposed further into  $TP_{major}$  and  $TP_{minor}$  parts as following equations.

$$\sigma = [TP_{minor} + TP_{major}] \\ = [TP_{minor} + 2^{-\omega}] \dots \dots \dots (b)$$

Compensation is planning for side effects or other unintended issues in a design. The design of an

invention can itself also be to compensate for some other existing issue or exception.

The compensation circuit is implemented to compute compensation bias based on

$$= [TP_{major} + TP_{minor}] \\ = [TP_{major} + 2^{-w}]$$

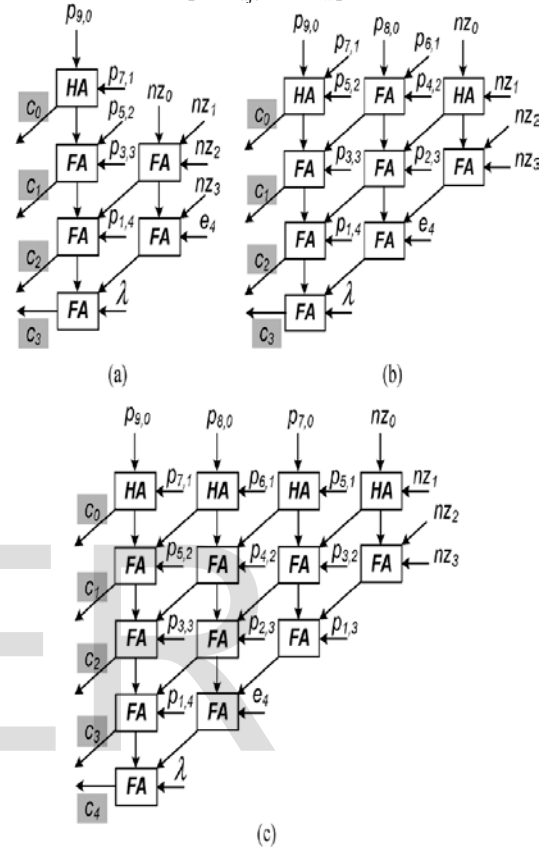


Fig1.5: Compensation circuits of ACPE Booth multipliers for  $w=1, 2, 3$ . (a)  $w=1$ . (b)  $w=2$ . (c)  $w=3$ .

**2.1 COMPENSATION CIRCUIT:**

Compensation is planning for side effects or other unintended issues in a design. The design of an invention can itself also be to compensate for some other existing issue or exception.

The compensation circuit is implemented to compute compensation bias based on

$$= [TP_{major} + TP_{minor}] \\ = [TP_{major} + 2^{-w}]$$

**2.2 CSA TREE:**

The carry-save adder generally consists of two ripple carry adders and a multiplexer. Adding two  $n$ -bit numbers with a carry-select adder is done

with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known.

The CSA tree and Brent-Kung parallel-prefix adder sum up the partial products of MP and based on

$$PP_q = MP + TP$$

$$= MP + .2^L$$

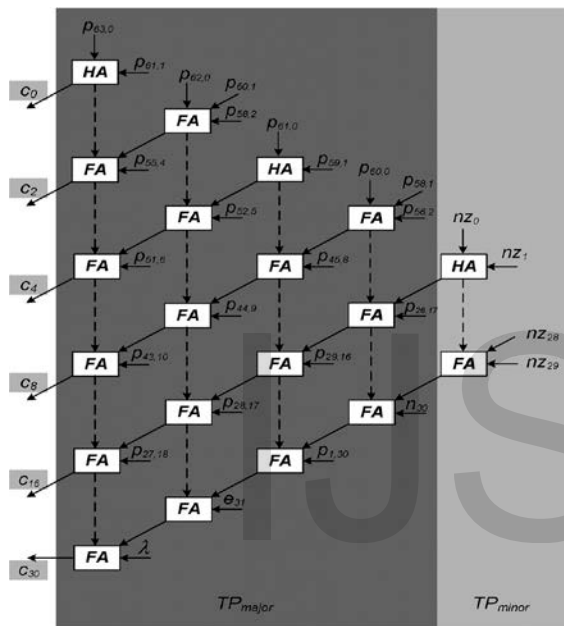


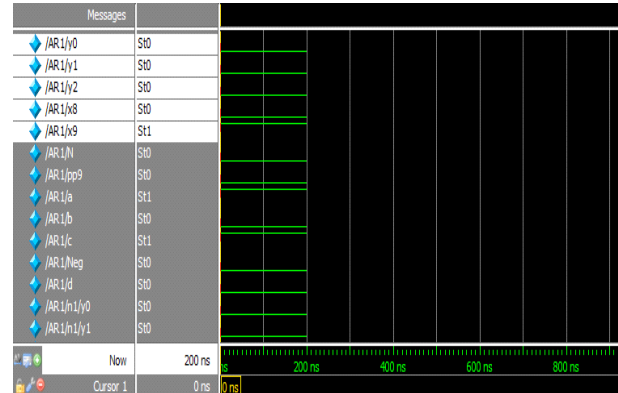
Fig1.6. The proposed 64-bit ACPE compensation circuit with w=4

### 3.RESULTS

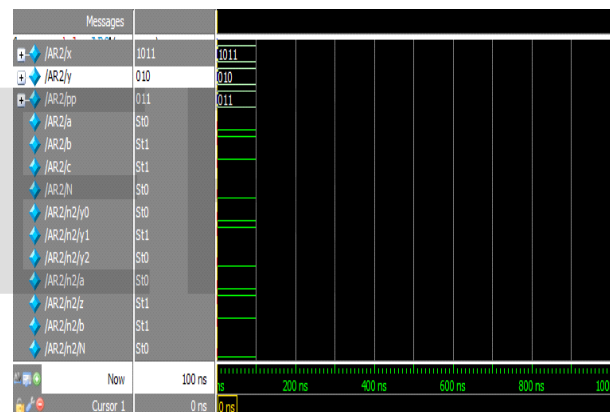
#### SIMULATION REPORTS

##### PARTITION OF TP w=1

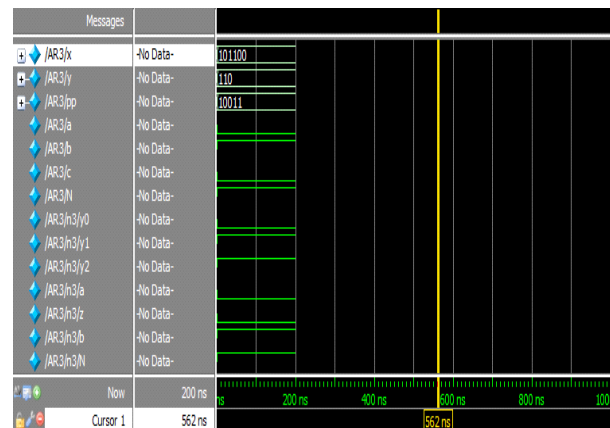
###### ROW1:



###### ROW2:



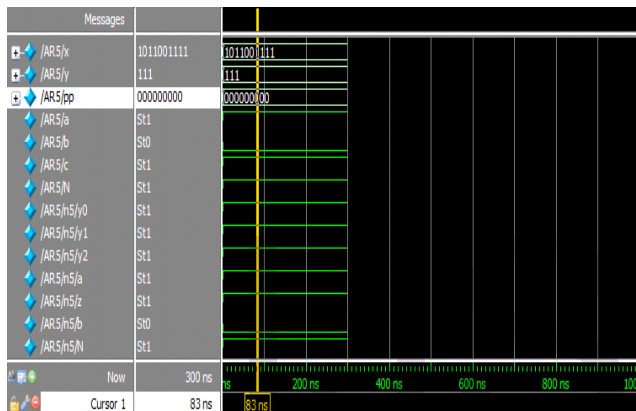
###### ROW3:



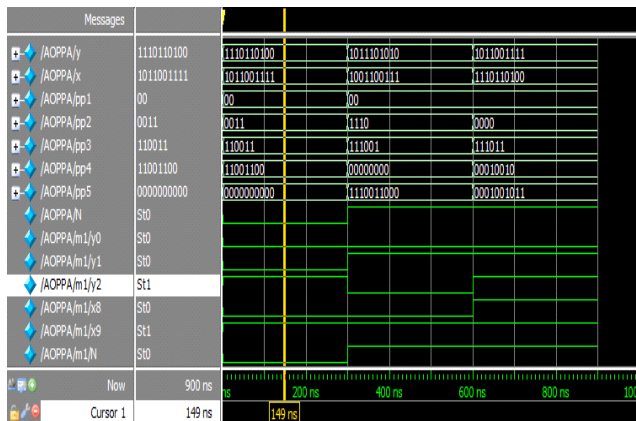
**ROW4:**



**ROW5:**

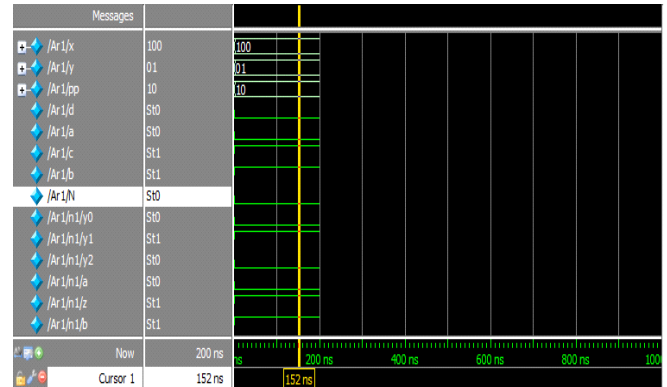


**OVER ALL PARTIAL PRODUCTS:**

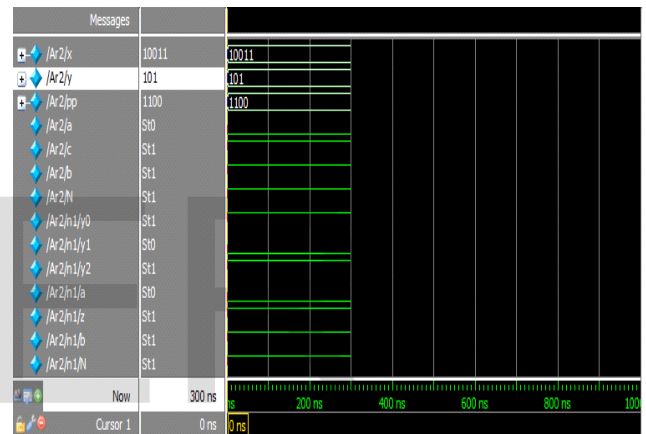


**3.1.2 PARTITION OF TP w=2:**

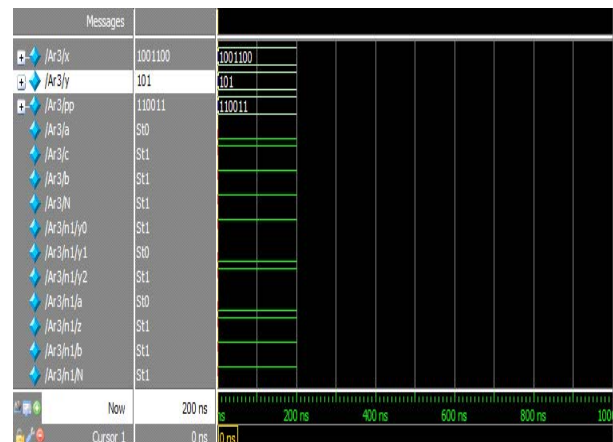
**ROW1:**



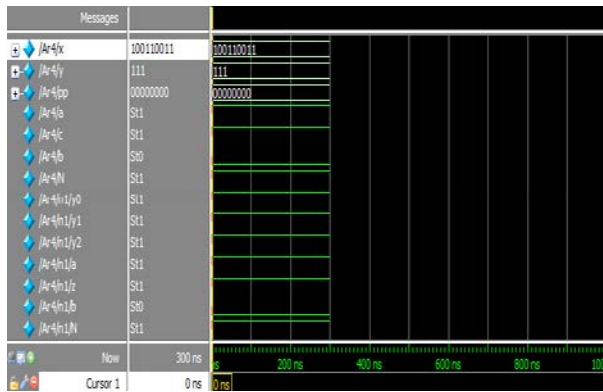
**ROW2:**



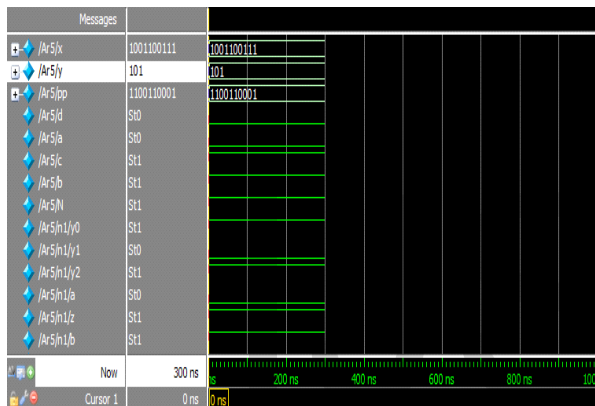
**ROW3:**



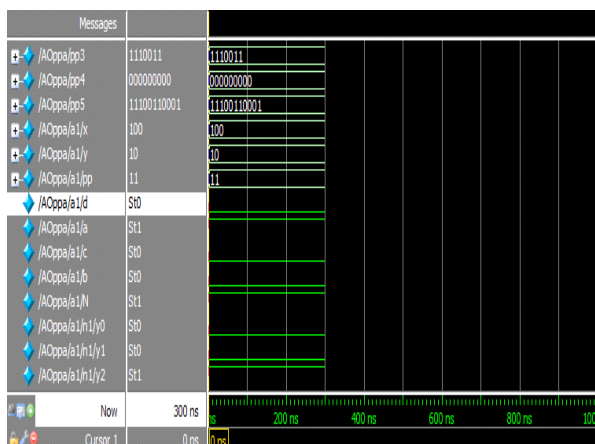
**ROW4:**



**ROW5:**

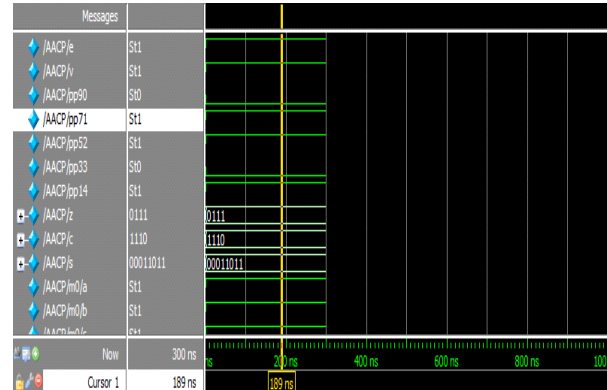


**OVER ALL PARTIAL PRODUCTS:**

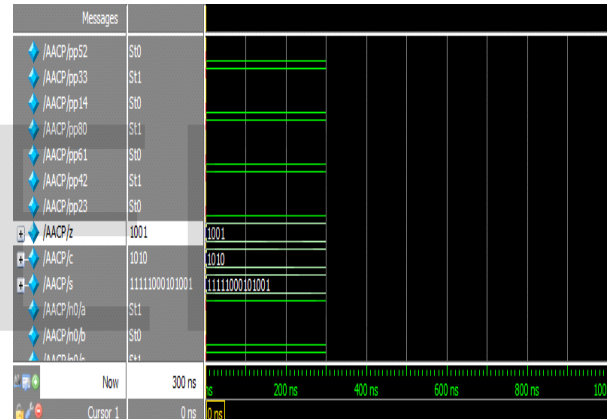


**3.2 COMPENSATION CIRCUIT**

**3.2.1 COMPENSATION W=1:**



**3.2.2 COMPENSATION w=2:**



**4. CONCLUSION**

This paper proposes an adaptive conditional-probability estimator (ACPE) in fixed-width Booth multipliers. Without heuristic method, the ACPE is derived from conditional-probability theory, which can be easily applied to large length Booth multipliers for achieving higher accuracy performance. The column information is also induced in ACPE to adjust the accuracy with respect to system requirements. For the 2-D DCT implementation with the ACPE Booth multipliers, an excellent performance is exhibited in terms of PSNR and area cost. As a result, the proposed ACPE provides a flexible and high accuracy compensation circuit applied to fixed-width Booth multipliers.

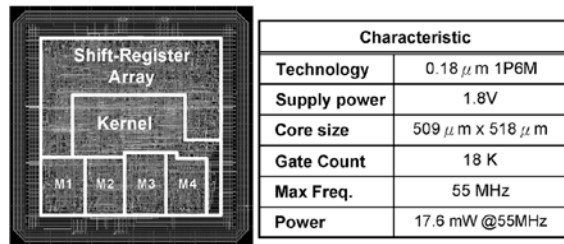


FIG. Core layout and characteristics of the proposed ACPE with  $\square$  applied in DCT core.

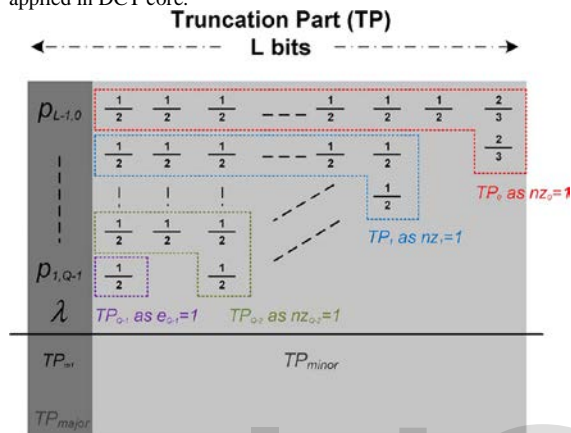


FIG. The conditional expected values of TP.

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